

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 2-21 are in this application. Claims 2, 4-5, 8, 10-11, and 13-14 have been amended. Claim 1 has been cancelled. Claims 15-21 have been added to alternately claim the present invention. In addition to the amendments discussed below, the claims have also been amended to add further clarity.

The Examiner rejected claim 14 under 35 U.S.C. §112, second paragraph. Specifically, the Examiner indicated that the claims did not appear to read on the disclosed invention. Claim 14, however, can be read onto applicant's FIG. 2. For example, the first and second transistors can be read to be transistors M4 and M7, respectively, and the third and fourth transistors can be read to be transistors M3 and M8, respectively. In addition, the fifth transistor can be read to be transistor Q2.

In this example, the third transistor (M3) pulls down an output voltage on an output node (OUTbar), the fourth transistor (M8) pulls down an intermediate voltage on a second intermediate node (base of Q2) to a second value. The falling second value turns on the fifth transistor (Q2) which then pulls down the output voltage on the output node (OUTbar). Thus, in view of the above, it is believed that claim 14 satisfies the requirements of the second paragraph of section 112.

Claims 2 and 8 were also amended to correct inadvertent errors in the connections of the seventh and tenth transistors. With respect to claim 2, the seventh transistor is now connected to the second output node, not the first output node. For example, following the amendment, the first transistor can be read to be transistor M3 shown in FIG. 2, the second transistor can be read to be transistor M4, the fifth transistor can be read to be transistor M7, the sixth transistor can be read to be transistor M9, and the seventh transistor can be read to be transistor Q1.

With respect to claim 8, the eighth transistor is now connected to the first output node, not the second output node. For example, following the amendment, the eighth transistor can be read to be transistor M8 shown in FIG. 2, the ninth transistor can be read to be transistor M10, and the tenth transistor can be read to be transistor Q2.

The Examiner rejected claims 1 and 13 under 35 U.S.C. §102(b) as being anticipated by applicant's FIG. 1. The Examiner also rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by Taub (U.S. Patent No. 6,385,099). The Examiner additionally rejected claims 1 and 13 under 35 U.S.C. §102(b) as being anticipated by Wang (U.S. Patent No. 6,414,534). The Examiner further rejected claims 1 and 13 under 35 U.S.C. §102(e) as being anticipated by Shimada et al. (U.S. Patent No. 6,750,696).

In addition, the Examiner rejected claims 1 and 13 under 35 U.S.C. §102(e) as being anticipated by Hayashi et al. (U.S. Patent No. 6,774,695). The Examiner further rejected claims 1 and 13 under 35 U.S.C. §102(e) as being anticipated by Aoki (U.S. Patent No. 6,717,453). The Examiner also rejected claim 1 under 35 U.S.C. §102(e) as being anticipated by Ziesler et al. (U.S. Patent No. 6,777,992). As noted above, claim 1 has been cancelled. Claim 13, in turn, has been amended to depend from allowable claim 2.

The Examiner objected to claims 2-12, but indicated that these claims would be allowable if amended to be in independent form and to include all of the limitations of the base claim and any intervening claims. Claim 2 has been amended to be in independent form, and is believed to include all of the limitations of claim 1. Claims 3-12 have not been amended to be in independent form as these claims depend either directly or indirectly from claim 2.

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Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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